CLAIMS

1. An output impedance bias compensation system for adjusting output impedance of at least one output, comprising:

a reference impedance generator that develops a reference impedance controlled by a reference impedance control input;

an impedance matching controller that continually adjusts said reference impedance control input to match said reference impedance with a reference value within a predetermined tolerance;

at least one output impedance generator, each coupled to a corresponding output and controlled by an output impedance control input; and

a programmable bias controller that combines a bias amount with said reference impedance control input to provide said output impedance control input.

2. The output impedance bias compensation system of claim 1, wherein said bias controller comprises:

output bias logic that is programmable to provide said bias amount; and

bias adjustment logic, coupled to said output bias logic and said impedance matching controller, that combines said bias amount with said reference impedance control input to provide said output impedance control input.

3. The output impedance bias compensation system of claim 2, wherein said output bias logic comprises a plurality of fuses.

4. The output impedance bias compensation system of claim 2, wherein said output bias logic comprises a programmable non-volatile logic device.

5. The output impedance bias compensation system of claim 2, wherein said bias amount comprises a signed bias value that is added to said reference impedance control input.

6. The output impedance bias compensation system of claim 2, wherein said bias amount comprises a signed percentage value indicative of a percentage of said reference impedance control input, and wherein said signed percentage value is added to said reference impedance control input.

7. The output impedance bias compensation system of claim 1, wherein said programmable reference impedance generator and each of said at least one programmable output impedance generator each comprise a binary array of matched devices.

8. The output impedance bias compensation system of claim 7, wherein said binary array of matched devices comprises matched P-channel pull-up devices.

9. The output impedance bias compensation system of claim 7, wherein said binary array of matched devices comprises matched N-channel pull-down devices.

10. An integrated circuit (IC) with output impedance adjustment, comprising:

a plurality of pins including a reference pin for coupling to an external reference resistor and at least one output pin;

at least one programmable output impedance generator, each controlled by an output impedance control input and coupled to a corresponding one of said at least one output pin; and

impedance matching logic, comprising:

a programmable reference impedance generator controlled by a reference impedance control input;

comparator logic that periodically adjusts said reference impedance control input to equalize values of said reference resistor and said programmable reference impedance generator within a predetermined tolerance; and

output adjustment logic that combines said reference impedance control input with a bias adjustment value to provide said output impedance control input.

11. The IC of claim 10, wherein said output adjustment logic comprises a plurality of programmable fuses.

12. The IC of claim 10, wherein said output adjustment logic comprises a programmable non-volatile logic device.

13. The IC of claim 10, wherein said programmable reference impedance generator and each said programmable output impedance generator comprises a binary array of matched impedance devices.

14. The IC of claim 10, wherein said bias adjustment value is added to or subtracted from said reference impedance control input.

15. The IC of claim 10, wherein said bias adjustment value comprises a percentage value indicative of a percentage of said reference impedance control input that is added to or subtracted from said reference impedance control input.

16. A method of adjusting output impedance of at least one output of an IC based on a reference impedance, comprising:

applying a reference voltage across the reference impedance and a reference impedance generator, the reference impedance generator having a reference impedance input;

adjusting the reference impedance input to equalize impedances of the reference impedance generator and the reference impedance within a predetermined tolerance;

measuring any difference between the reference impedance and at least one output impedance;

programming a nonvolatile device on the IC with a bias adjust value to compensate for any measured difference; and

combining the bias adjust value with the reference impedance input to provide an output impedance input of at least one output impedance generator, each output impedance generator coupled to a corresponding output.

17. The method of claim 16, wherein said programming a bias adjust value comprises blowing at least one fuse.

18. The method of claim 16, wherein said programming a bias adjust value comprises programming at least one bit of a non-volatile memory.

19. The method of claim 16, wherein said bias adjust value comprises a signed bias value, and wherein said combining the bias adjust value with the reference impedance input comprises adding the signed bias value.

20. The method of claim 16, wherein said bias adjust value comprises a percentage value indicative of a percentage of the reference impedance input and a polarity signal, and wherein said combining the bias adjust value with the reference impedance input comprises adding the percentage to or subtracting the percentage from the reference impedance input based on the polarity signal.